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CLAIMS

[Claim(s)]

[Claim 1] Two or more photosensitive picture elements which generate the signal charge according to the amount of incident light, and the shift register which generates a predetermined control pulse based on the pulse inputted from the outside, Two or more charge electrical-potential-difference conversion means established corresponding to each of two or more of said photosensitive picture elements, It comes to integrate common output Rhine which unifies the output of two or more of said charge electrical-potential-difference conversion means, and is outputted outside on a semi-conductor substrate. Said charge electrical-potential-difference conversion means The charge storage section which accumulates the signal charge which the corresponding photosensitive picture element generated, and a reset pulse generation means to generate a reset pulse based on the control pulse sent out from the pulse inputted from the outside, and said shift register, The reset gate which opens and closes the gate based on the reset pulse which is adjoined and prepared in said charge storage section, and is sent out from said reset pulse generation means, The reset drain which sets said charge storage section as predetermined potential when said reset gate opens, The current source connected to the serial between the 1st driver gate where the potential of said charge storage section is impressed, this 1st driver gate, and an earth terminal, The switch gate for power-source closing motion connected to a serial between said 1st driver gate and power supply terminals, The charge detecting element which an end is connected to a power supply terminal, and the other end is connected to said common output Rhine, has the 2nd driver gate where the electrical potential difference of the node of said 1st driver gate and said current source is impressed, and detects the charge of said charge storage section, It is based on the predetermined control pulse which a preparation and said shift register generate. The solid state camera characterized by detecting the amount of integrals of the signal charge which a corresponding photosensitive picture element generates, and the zero reference level of this amount of integrals, changing these detection values into an electrical potential difference, and sending out to said common output Rhine alternatively.

[Claim 2] The solid state camera according to claim 1 characterized by connecting one source of the load current to said common output Rhine, and coincidence integrating on a semi-conductor substrate.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[Objects of the Invention]

(Field of the Invention)

This invention relates to a solid state camera.

(Prior art)

The contact type image sensor using CCD linear image sensors or an amorphous silicon as conventional linear image sensors is used.

(Object of the Invention)

In the case of an above-mentioned CCD sensor, since read-out of a signal is generally performed using the CCD analog shift register, a production process is complicated, and it had the trouble that driver voltage was high compared with an amorphous sensor, with the trouble of not being cheap.

On the other hand, in the case of the contact type image sensor using an amorphous silicon, since an output was obtained in the form of a photocurrent, there was a trouble that sufficient S/N ratio was not obtained while making the suitable integrator outside attachment.

This invention is made in consideration of the above-mentioned trouble, and is easy a production process, and it aims at offering the solid state camera which can obtain sufficient S/N ratio.

[Elements of the Invention]

(Means for solving a trouble)

Two or more photosensitive picture elements with which the solid state camera by this invention generates the signal charge according to the amount of incident light, The shift register which generates a predetermined control pulse based on the pulse inputted from the outside, Two or more charge electrical-potential-difference conversion means established corresponding to each of two or more of said photosensitive picture elements, It comes to integrate common output Rhine which unifies the output of two or more of said charge electrical-potential-difference conversion means, and is outputted outside on a semi-conductor substrate. Said charge electrical-potential-difference conversion means It is characterized by detecting the amount of integrals of the signal charge which a corresponding photosensitive picture element generates, and the zero reference level of this amount of integrals based on the predetermined control pulse

which said shift register generates, changing these detection values into an electrical potential difference, and sending out to said common output Rhine alternatively.

(Operation)

Thus, according to the solid state camera by constituted this invention, since read-out of a signal charge is performed based on a predetermined control pulse, unlike the conventional CCD sensor, formation of multilayer polish recon becomes unnecessary and a production process becomes easy. Moreover, the amount of integrals of a signal charge and the zero reference level of this amount of integrals are detected by the charge electrical-potential-difference conversion means, are changed into a corresponding electrical-potential-difference value, and are alternatively outputted outside through common output Rhine. Processing of a correlation duplex sampling for example, etc. is attained by this, and sufficient S/N ratio can be obtained.

(Example)

The example of this invention is explained using a drawing. In Fig. 1, a sign 1 is a semi-conductor substrate and a shift register 2, a photosensitive picture element PE 1,PE_n, the charge electrical-potential-difference conversion means A₁, ..A_n, a current source 4, and common output Rhine 5 are integrated by this semi-conductor substrate 1. Moreover, Terminals 8a, 8b, 8c, 8d, 8e, 8f, and 8g are formed in the semi-conductor substrate 1. Driving pulses phi1 and phi2 are regularly impressed to a shift register 2 through Terminals 8a and 8b, respectively from the exterior. Furthermore, start pulse phi* is impressed to a shift register 2 through terminal 8c, and direct current voltage (for example, 5V) is impressed to a shift register 2 and the charge electrical-potential-difference conversion means A₁,A_n through 8d of terminals. Moreover, reset pulse phiR inputted through terminal 8e is impressed to the charge electrical-potential-difference conversion means A₁ andA_n. In addition, 8f of terminals is an earth terminal.

On the other hand, based on driving pulses phi1 and phi2 and start pulse phi*, a shift register 2 generates control pulse phisi and phiBi (i= 1,n), and sends them out to the charge electrical-potential-difference conversion means A_i. Thus, one example of the shift register 2 which generates control pulse phisi and phiBi (i= 1,n) based on driving pulses phi1 and phi2 and start pulse phi* is shown in Fig. 5. The shift register 2 consists of the start circuit SR 0, n control pulse generating circuits SR 1,SR_n in Fig. 5. The start circuit SR 0 consists of four MOS transistors (only henceforth a transistor) M01,M04 and the capacity C0 of one piece, as shown in Fig. 5. Moreover, the control pulse generating circuit SR_i (i= 1,n) consists of eight MOS transistors Mi1, ..Mi8 and the capacity Ci1 and Ci2 of two pieces, as shown in Fig. 5.

In addition, in Fig. 5, four MOS transistors M25 of the control pulse generating circuit SR 2 </SUB>, and M26, M27, M28 and capacity C22 are omitted.

Next, actuation of the start circuit SR 0 and the control pulse generating circuit SR_i is explained using Fig. 6.

When the driving pulses phi1 and phi2 shown in [Fig. 6](#) are impressed to the shift register 2, the case where start pulse phi* is impressed in time of day t1 is considered. The direct current voltage of 5V is impressed to the source side of MOS transistor M01 of the start circuit SR 0 through 8d of terminals shown in [Fig. 1](#). If start pulse phi* is impressed to the gate of MOS transistor M01 in time of day t1, potential phia of the point a by the side of the drain of a transistor M01 will go up from a low, and will become a certain value not more than 5V. And in time of day t2, the level of start pulse phi* turns into a low from a high level, and potential phia of Point a has become as [a certain value not more than 5V] under the effect of capacity C0. Although this potential phia is impressed to the gate of a transistor M02, since the level of a driving pulse phi 2 is a low, potential phib of Point b is also a low. This condition continues until the level of a driving pulse phi 2 becomes quantity from low in time of day t4.

If the level of a driving pulse phi 2 becomes quantity from low in time of day t4, potential phib of Point b will become the existing value beyond 5V, as it goes up, therefore potential phia of Point a also goes up by the vasopressor action and it is shown in [Fig. 6](#). And this condition continues till time of day t5. If time of day t5 comes, since the level of a driving pulse phi 2 will become low from quantity, potential phib of Point b also becomes low from quantity, therefore potential phia of Point a also falls to a certain value not more than 5V from the existing value beyond 5V.

On the other hand, the direct current voltage of 5V is impressed to the source side of the transistor M11 of the control pulse generating circuit SR 1 through 8d of terminals shown in [Fig. 1](#). Since potential phib is impressed to the gate of a transistor M11, potential phic of the point c by the side of the drain of a transistor M11 as well as the case of potential phia of the point a of the start circuit SR 0 goes up from a low to a certain value not more than 5V in time of day t4. And this condition continues till the time of day t6 when the level of the driving pulse phi 1 impressed to the source side of a transistor M12 becomes quantity from low. Since potential phic is impressed to the gate of a transistor M12 and the level of a driving pulse phi 1 becomes quantity from low at time of day t6, potential phid of Point d goes up. Therefore, by the vasopressor action, potential phic of Point C also goes up and it becomes the existing value beyond 5V. And this condition continues till the time of day t7 when the level of a driving pulse phi 1 becomes low from quantity.

In addition, since potential phid changes from a low to a high level in time of day t6, the gate of the transistor M03 of the start circuit SR 0 where this potential phid is impressed is opened in time of day t6, and potential phia of Point a is set to a low.

If time of day t7 comes, since the level of a driving pulse phi 1 becomes low from quantity, potential phid of Point d will also be set to a low from a high level, therefore potential phic of Point c will also fall to a certain value not more than 5V from the existing value beyond 5V.

On the other hand, the direct current voltage of 5V is impressed to the source side of the

transistor M15 of the control pulse generating circuit SR 1 through 8d of terminals shown in [Fig. 1](#) , and since potential phid is impressed to the gate of a transistor M15, potential phie of the point e by the side of the drain of a transistor M15 goes up from a low to a certain value not more than 5V in time of day t6. And this condition continues till the time of day t8 when the level of the driving pulse phi 2 impressed to the source side of a transistor M16 becomes quantity from low. Since potential phie is impressed to the gate of a transistor M16 and the level of a driving pulse phi 2 becomes quantity from low at time of day t8, potential phif of Point f goes up. Therefore, by the vasopressor action, potential phie of Point e also goes up and it becomes the existing value beyond 5V. And this condition continues till the time of day t9 when the level of a driving pulse phi 2 becomes low from quantity.

In addition, since the level of potential phif of Point f becomes quantity from low in time of day t8, the gate of a transistor M13 where this potential phif is impressed is opened in time of day t8, and potential phic of Point c is set to a low. And potential phic and phif are taken out from the control pulse generating circuit SR 1 as a control pulse phis1 and phiB1, respectively, and are sent out to the charge electrical-potential-difference conversion means A1.

In addition, potential phif is impressed to the gate of the transistor M21 of the control pulse generating circuit SR 1 to a control pulse generating circuit, a control pulse phis2 and phiB-2 are taken out from the control pulse generating circuit SR 2 like the case where it is the control pulse generating circuit SR 1, and it is sent out to the charge electrical-potential-difference means A2. By repeating such a thing successively, control pulse phiSi and phiBi are taken out from the control pulse generating circuit SRI ($i = 1, \dots, n$), and it is sent out to the charge electrical-potential-difference conversion means Ai. In addition, control pulse phiSi serves as 3 value pulse, as shown in [Fig. 6](#) , and the record level is higher than supply voltage (5V).

Again, in [Fig. 1](#) , based on reset pulse phiR impressed through control pulse phiSi, phiRi, and terminal 8e, the charge electrical-potential-difference conversion means Ai ($i = 1, \dots, n$) detects the amount of integrals of the signal charge which a photosensitive picture element PEi generates, and the zero reference level of this amount of integrals, changes these detection values into an electrical potential difference, and sends them out to common output Rhine 5 alternatively. And the output Vout of the charge electrical-potential-difference conversion means Ai sent out alternatively is outputted to common Rhine 5 outside through 8g of terminals.

One example of such a charge electrical-potential-difference conversion means Ai is shown in [Fig. 2](#) . A sign 11 shows the capacity which accumulates the signal charge generated in the photosensitive picture element (for example, photodiode) PEi, and a sign 12 shows a reset transistor. Signs 14-19 show an MOS transistor (only henceforth a transistor), and a sign 20 shows a current source. A sign 21 shows the driver gate and a sign 24 shows the capacity for pressure ups.

And control pulse phiSi is impressed to the gate of transistors 15 and 18, as shown in Fig. 2 , and control pulse phiBi is impressed to the gate of a transistor 17. Moreover, reset pulse phiR is impressed to the source of a transistor 16.

In addition, Photodiode PEi is constituted by forming P well on a n-type-semiconductor substrate, as shown in Fig. 3 , and forming n field and P+ field in the front face of this P well.

Moreover, two n+ fields are separated and formed in the front face of P well, and one of n+ fields [them] touches n field. The reset transistor 12 is constituted by the electrode formed between this n+ field and the two above-mentioned n+ fields.

Actuation of the charge electrical-potential-difference conversion means Ai shown in Fig. 2 is explained using Fig. 4 . Reset pulse phiR shown in Fig. 4 and control pulse phiSi, and phiBi shall be impressed to the charge electrical-potential-difference conversion means Ai. In addition, it is cautious of having generated control pulse phiSi and phiBi repeatedly the same period as the period of start pulse phi* of a shift register. The direct current voltage of 5V is impressed to the source and the gate of a transistor 14 through 8d of terminals shown in Fig. 1 (refer to the 2nd Fig.). And in time of day T1, if control pulse phiSi is impressed to the gate of a transistor 15, potential phialpha of the point alpha shown in Fig. 2 will go up a little from a low, and will be set to a certain predetermined level (refer to the 4th Fig.). Since the level of control pulse phiSi becomes quantity in time of day T2, potential phialpha is set to standby level. And if it becomes time-of-day T3, since the level of reset pulse phiR will become quantity from low, by the vasopressor action, potential phialpha of Point alpha also goes up and it is set to a certain predetermined level (this level is hereafter called reset level). Next, if it becomes time-of-day T four, since the level of reset pulse phiR will become low from quantity, potential phialpha is again set to standby level. And this standby level continues till time of day T5.

Thus, pulse phiRSi (=phialpha) impressed to the gate of the reset transistor 12 serves as 4 value pulse. And capacity 11 holds the signal charge during the period whose pulse phiRSi is standby level, without being reset by the reset transistor 12. Capacity 11 is reset by time-of-day T3 from which pulse phiRSi is set to reset level. And this reset condition continues to time-of-day T four. Potential phibeta of the point beta shown in Fig. 2 falls as the signal charge from Photodiode PEi is accumulated in capacity 11 after that.

When the level of control pulse phisi is a record level (from time of day T2 up to T5), a transistor 19 is activated as a source follower circuit. In the period whose level of control pulse phisi the level of pulse phiRSi is standby level, and is the maximum level, potential phigamma corresponding to the amount of the signal charge accumulated in capacity 11 by time of day T2 after the last reset action (from time of day T2 to T3) is detected in a source follower circuit. And potential phibeta of capacity 11 is reset in the time amount whose level of control pulse phisi the level of pulse phiRSi is reset level,

and is the maximum level (from time-of-day T3 to T four). Moreover, in the period whose level of control pulse phisi the level of pulse phiRSi is standby level, and is the maximum level, the potential of the capacity 11 in the condition that there is almost no signal charge in case a signal charge starts an inflow from the photodiode PEi after reset (from time-of-day T four to T5) is detected. It can be considered that the level at this time is the zero criteria of a signal charge.

And detected potential phigamma is amplified by the driver gate 21, and is sent out to common output Rhine 5. In addition, before control pulse phisi is impressed to the gate of a transistor 18, potential phigamma of Point gamma is zero, and since this potential phigamma is impressed to the driver gate 21, common output Rhine 5 is not influenced of the potential of Point gamma. Moreover, since the level of control pulse phisi impressed to other n-1 charge electrical-potential-difference conversion means A_j ($j \neq i$) is a low when potential phigamma of the point gamma of the charge electrical-potential-difference conversion means A_i is not zero (i.e., when control pulse phisi is not a low), the output of other n-1 charge electrical-potential-difference conversion means A_j will be intercepted. Therefore, in common output Rhine 5, read-out of potential, i.e., a signal charge, becomes possible alternatively.

Since read-out of a signal charge is performed by the above based on a predetermined control pulse according to this example, unlike the conventional CCD sensor, formation of multilayer polish recon becomes unnecessary and a production process becomes easy. Moreover, by changing the amount of integrals of a signal charge, and the zero reference level of this amount of integrals into an electrical-potential-difference value, and outputting them outside alternatively through common output Rhine 5, processing of a correlation duplex sampling for example, etc. is attained, and sufficient S/N ratio can be obtained. Furthermore, it can drive with a low battery called 5V.

[Effect of the Invention]

As stated above, according to the solid state camera of this invention, a production process can obtain sufficient S/N ratio easily.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

The block diagram showing the example of the solid state camera according [Fig. 1] to this invention, the circuit diagram showing the configuration of the charge electrical-potential-difference conversion means which Fig. 2 requires for the solid state camera of this invention, The timing chart explaining actuation of the charge electrical-potential-difference conversion means which shows drawing showing the structure of the photosensitive picture element which Fig. 3 requires for the solid state

camera of this invention, and Fig. 4 in Fig. 2 , The circuit diagram showing the configuration of the shift register which Fig. 5 requires for the solid state camera of this invention, and Fig. 6 are the timing charts explaining actuation of the shift register shown in Fig. 5 .

1 [.. Common output Rhine, 8a, 8b, 8c, 8d 8e, 8f, 8g / .. A terminal, PEi (i= 1, ..n) / .. A photosensitive picture element, Ai (i= 1, ..n) / .. Charge electrical-potential-difference conversion means.] A semi-conductor substrate, 2 .. A shift register, 4 .. A current source, 5